

FIG 1

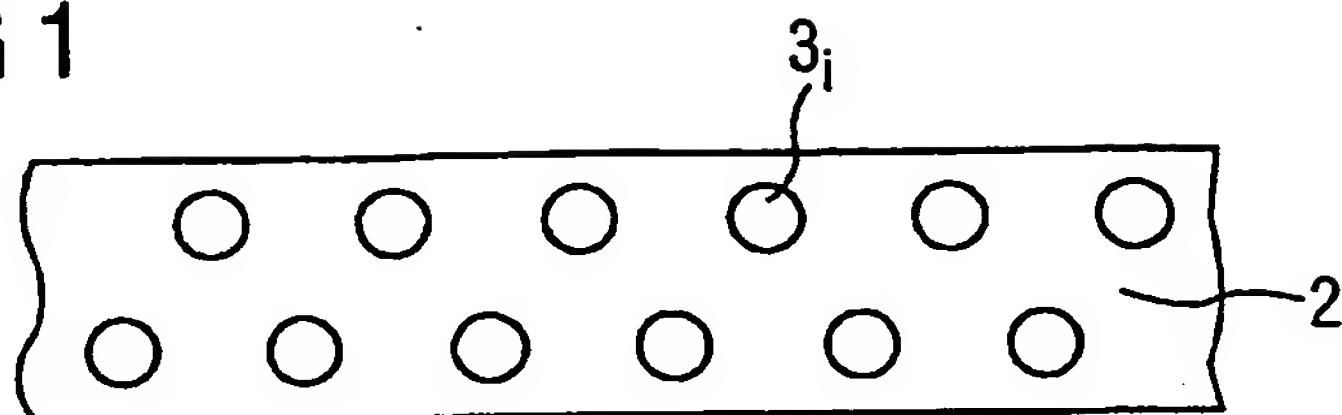


FIG 2

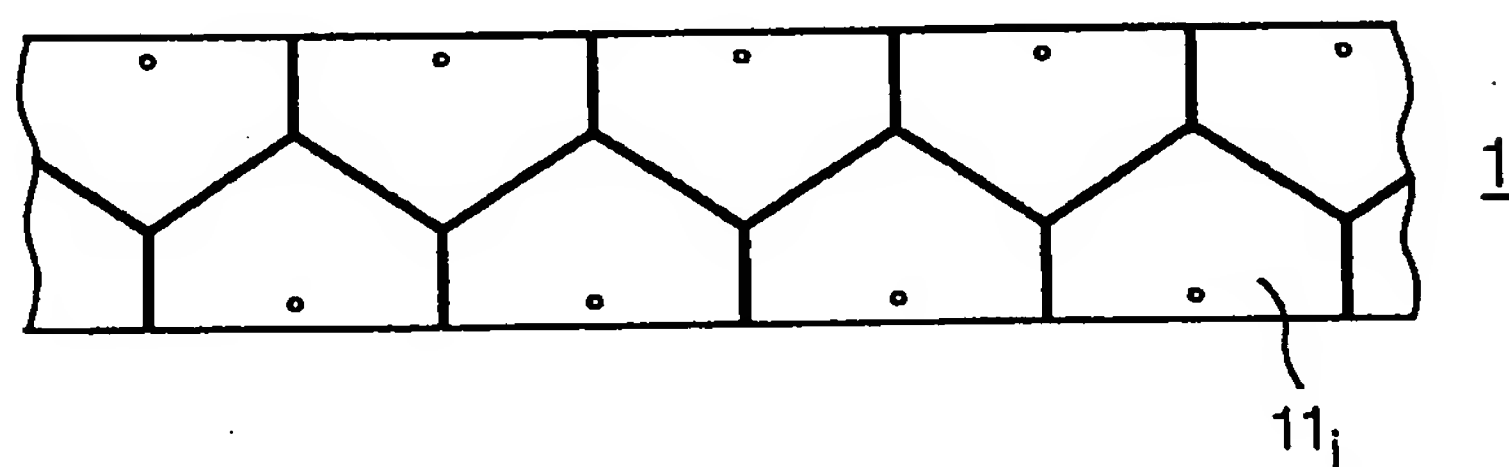


FIG 3

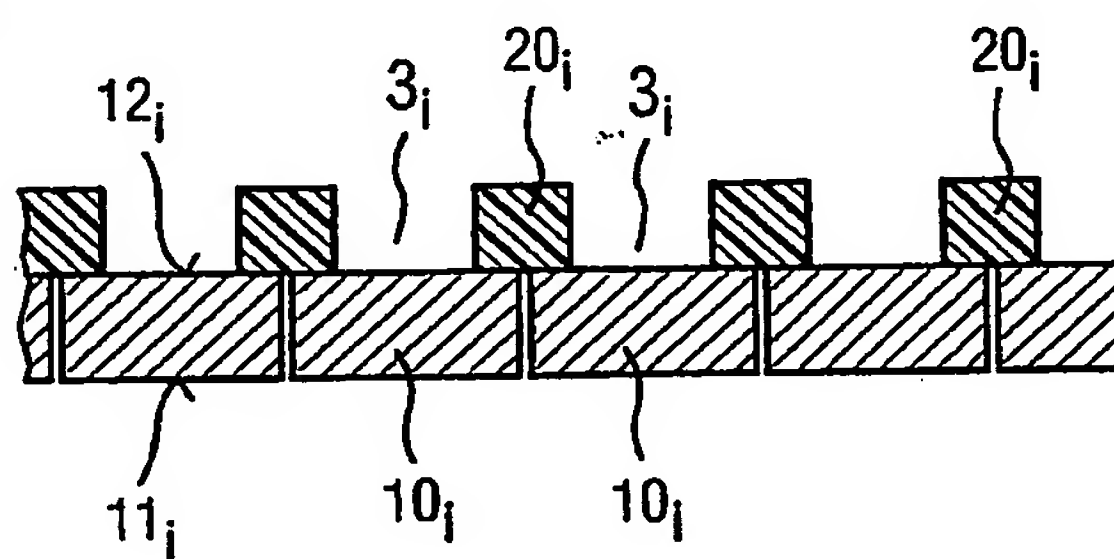


FIG 4

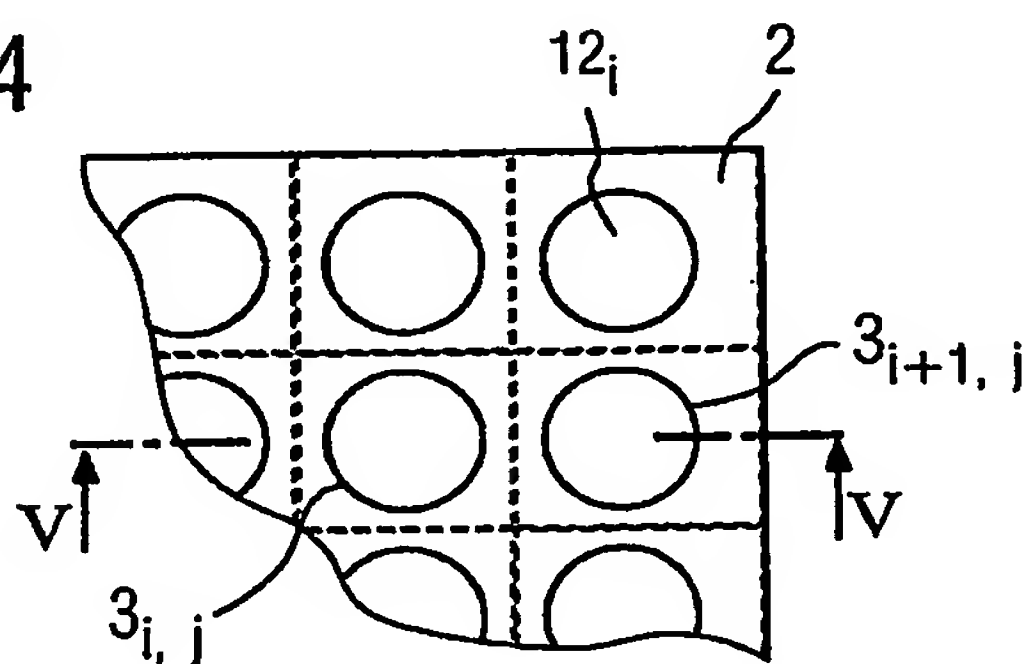


FIG 5

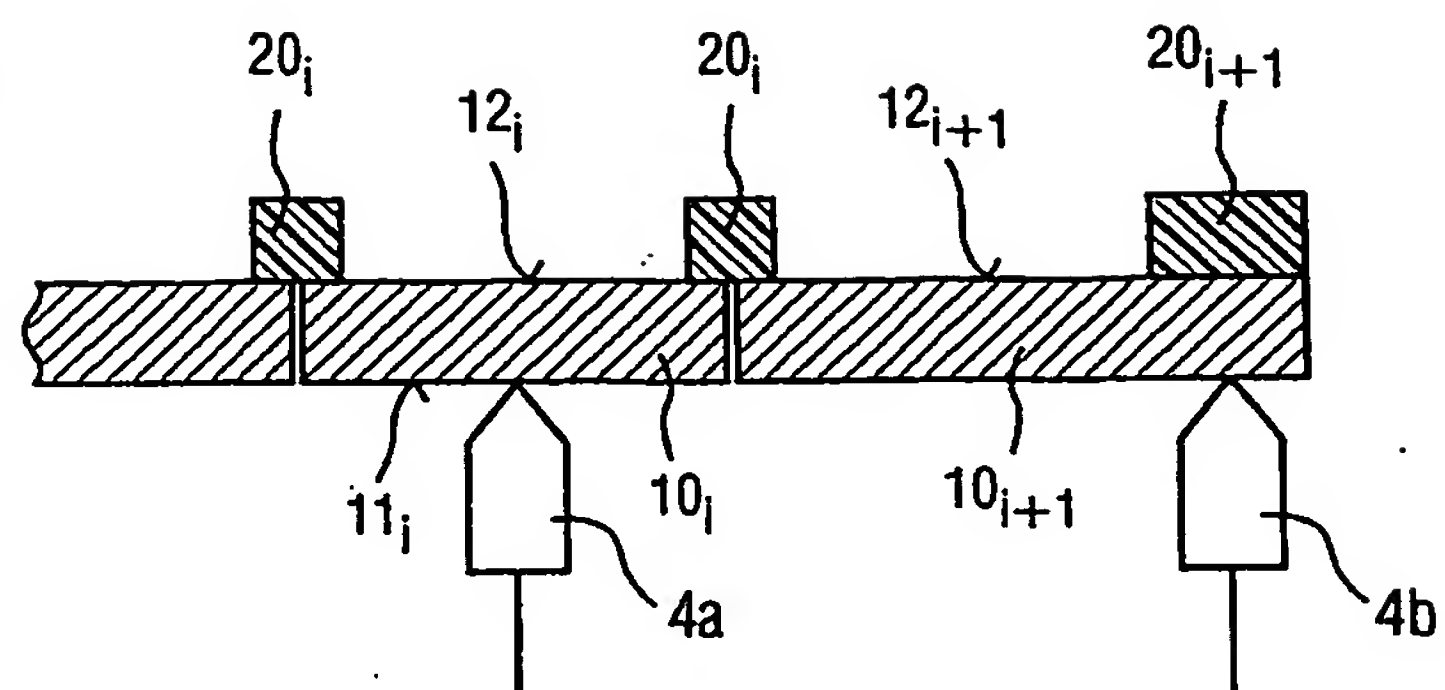


FIG 6

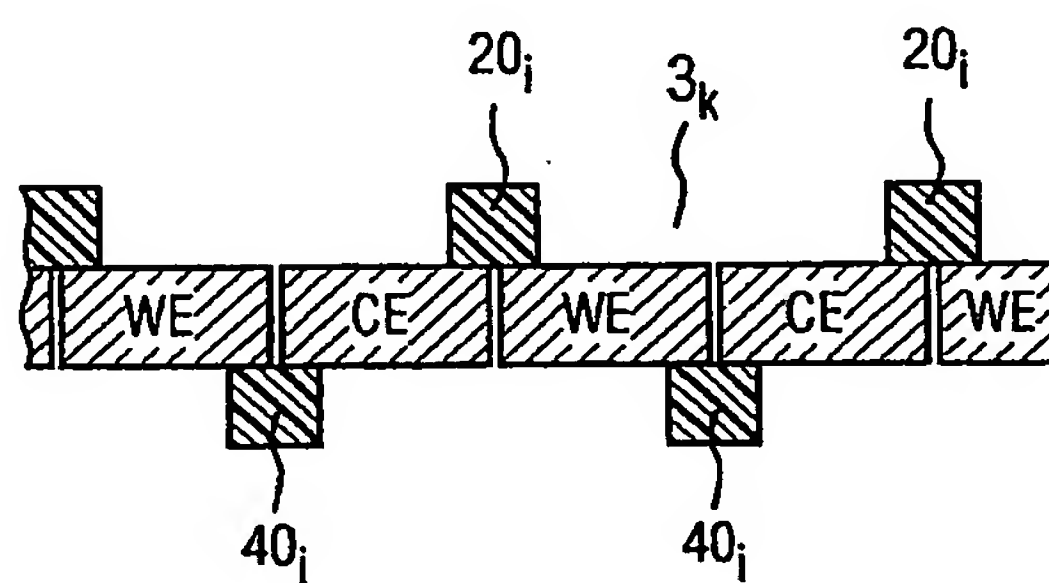


FIG 7

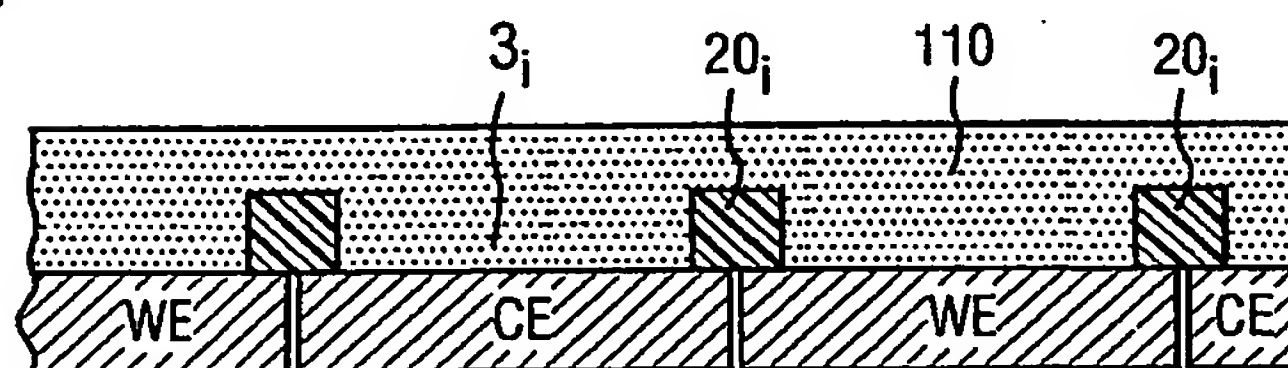


FIG 8

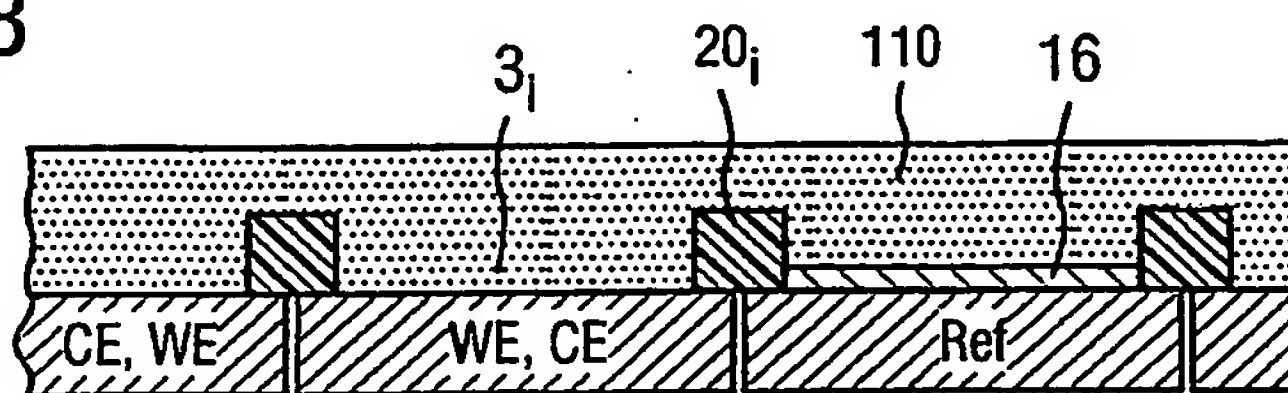


FIG 9

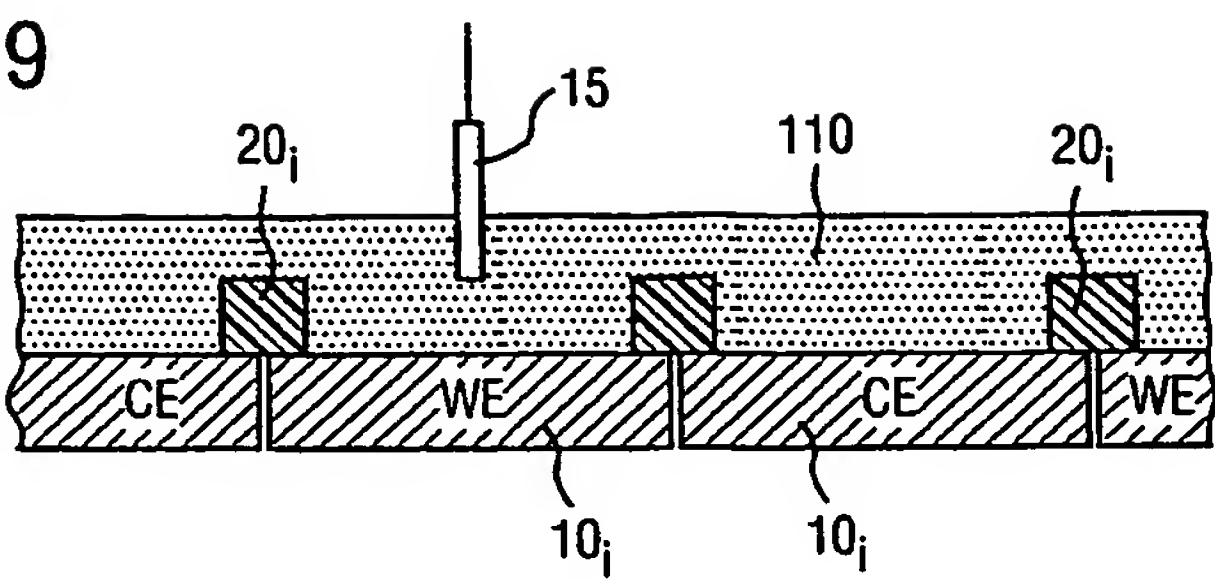


FIG 10

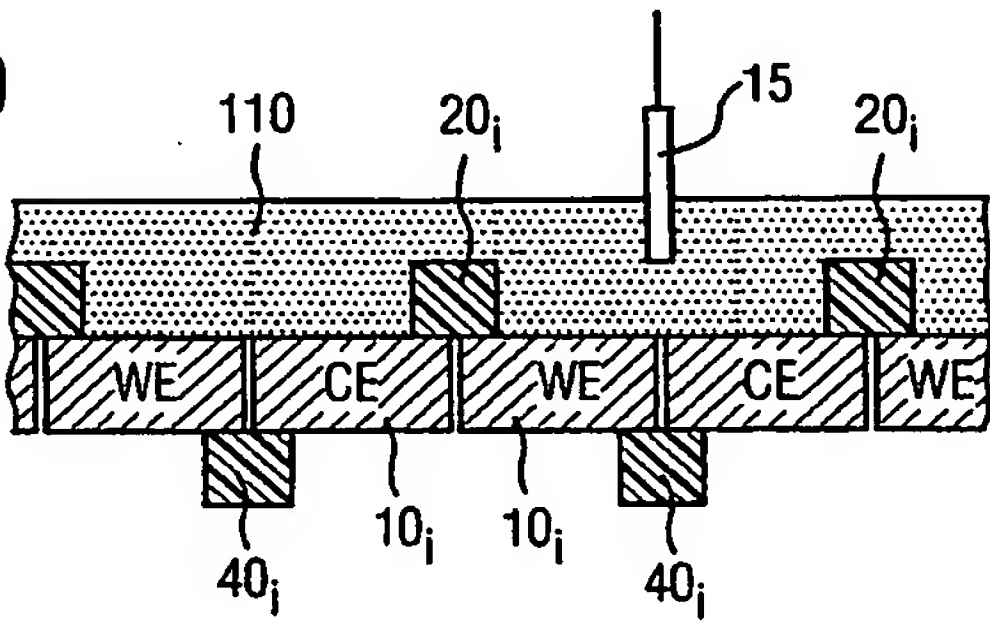


FIG 11

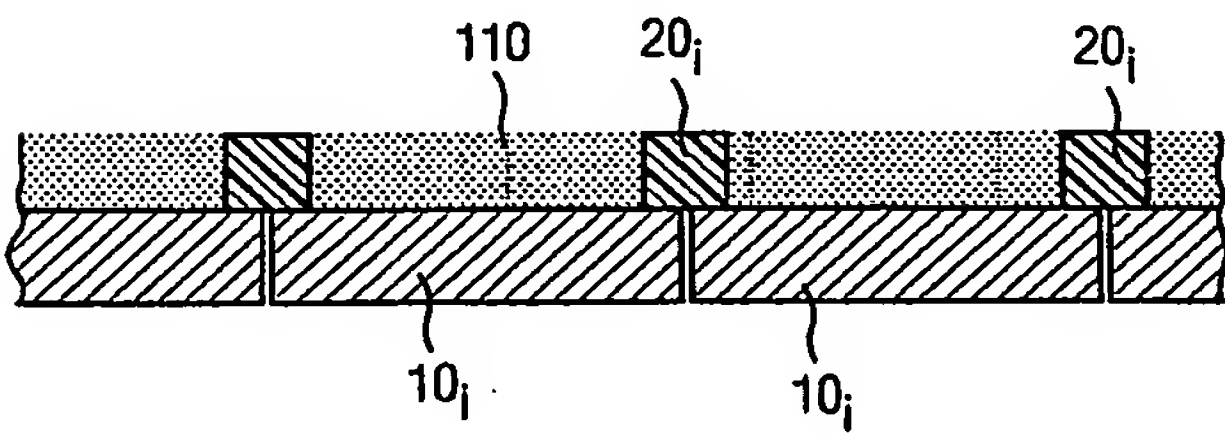


FIG 12

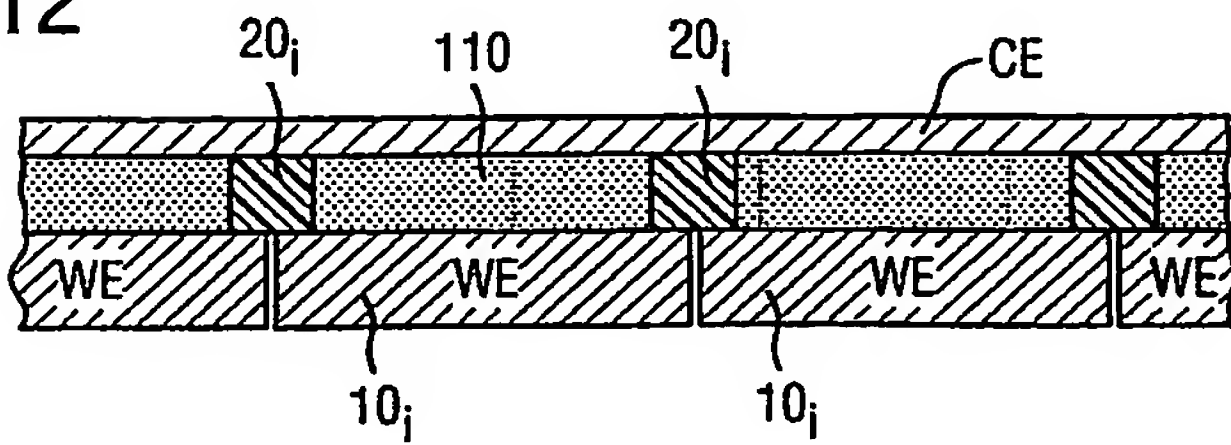


FIG 13

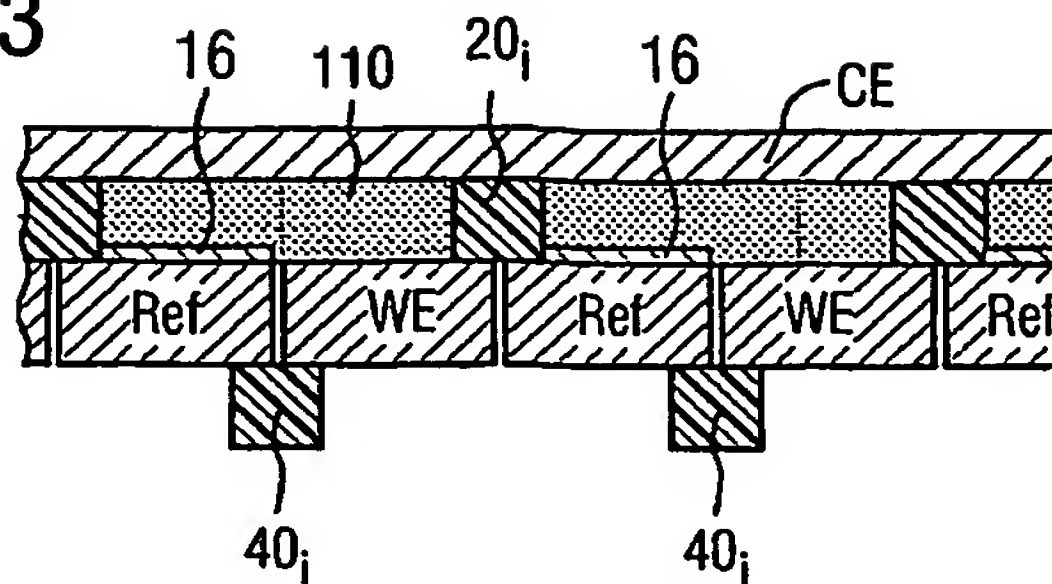


FIG 14

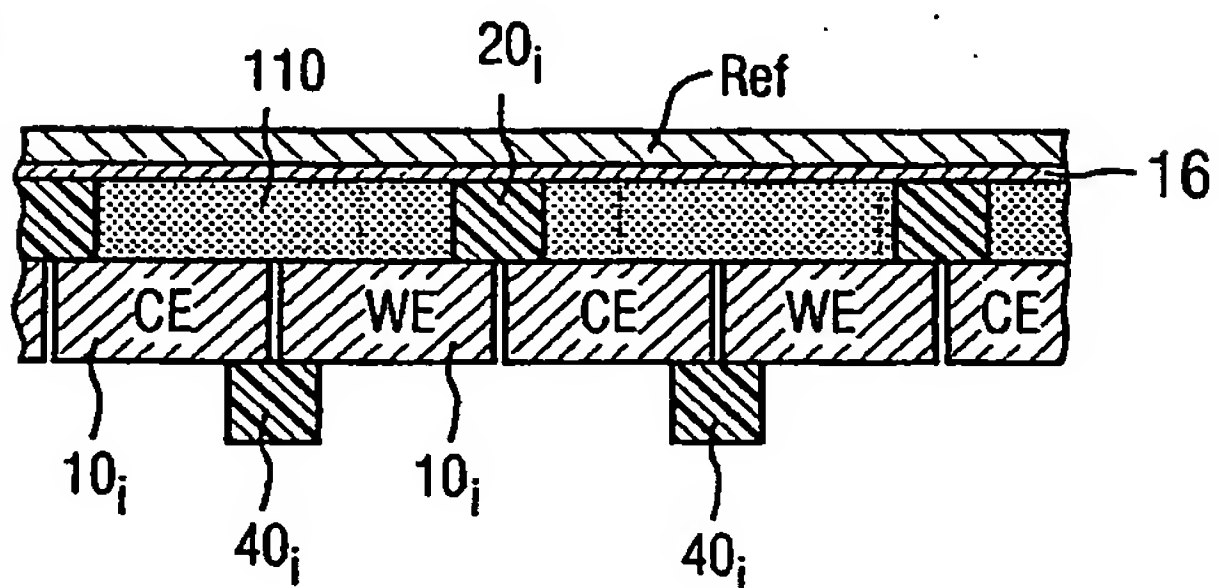


FIG 16

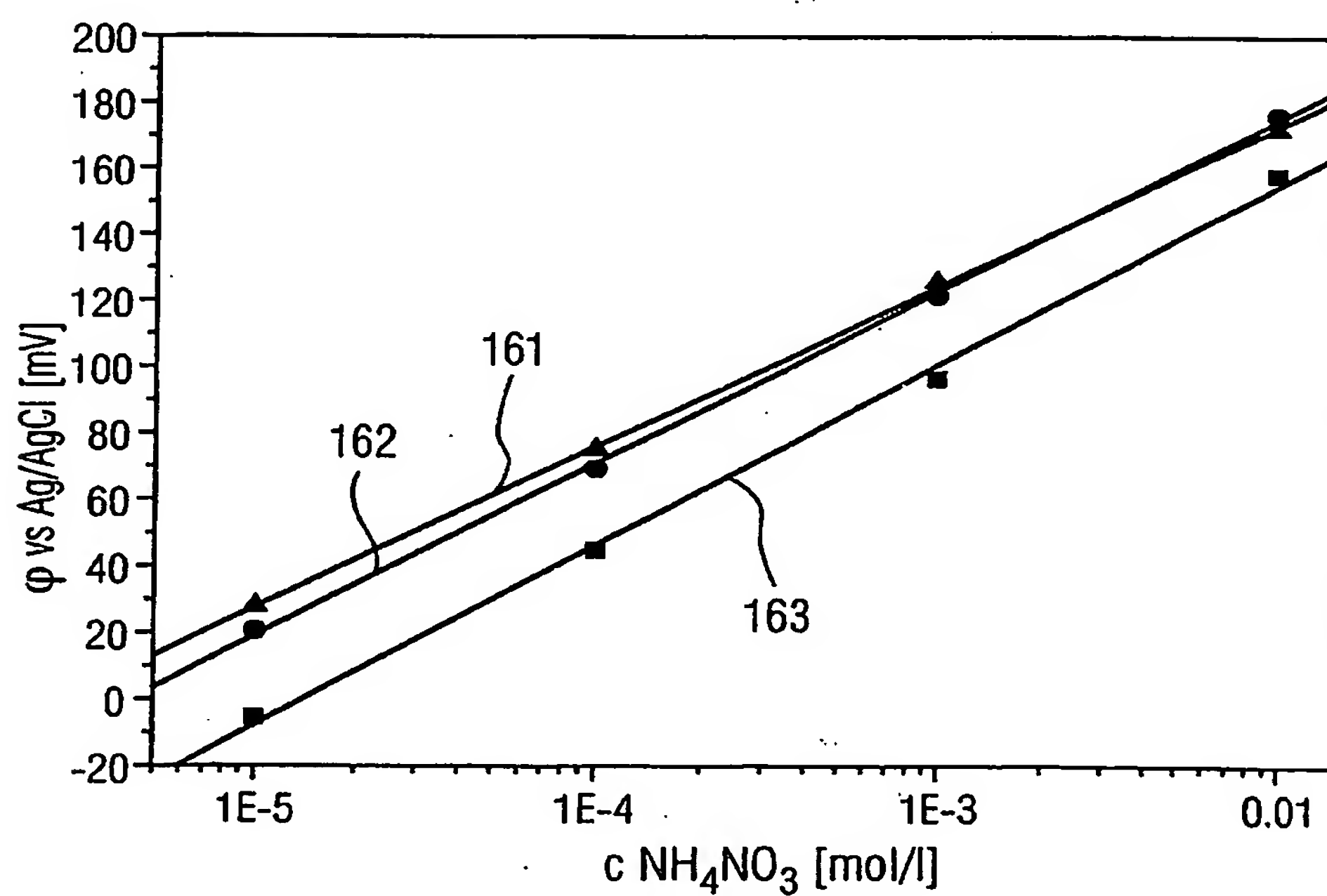


FIG 15

FIG 15 is a schematic diagram of a memory array structure and its electrical circuit. The top part shows a cross-section of a memory array with layers 100, 110, 12_i, 11_i, 10_i, 3_i, and 20_i. It includes control lines CE (4c), Ref (4b), and WE (4a). The bottom part shows a circuit with a square wave generator 6, an op-amp 7, a resistor 8, and another op-amp 7'. The output is a plot of $U_{out} \sim I$ versus time t , showing a series of pulses.

FIG 17

